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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,772	08/25/2003	Milivoje Aleksic	00100.03.0009	2757

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EXAMINER	
CHAUHAN, ULKA J	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,772	ALEKSIC ET AL.	
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-4, 6-9, 10-13, 15-17, 19-21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,342,892 to Van Hook et al and U.S. Patent No. 6,762,763 to Migdal et al.

4. As per claim 1, Van Hook teaches a high performance 3D graphics system comprising: a command queue capable of receiving a plurality of rendering commands (Fig. 20: *command unit buffer RAM 516*; c. 49 ll. 17-19: *once one or more commands have been loaded into command unit buffer RAM 516...*), a generate_event command (c. 48 ll. 27-30: *display processor 500 obtains data for its texture memory 502 by passing texture load commands to command unit 514 and using memory interface 512 to perform those commands*);

a direct memory access device coupled to the command queue (Fig. 20: *DMA controller 518 coupled to the command unit 514 including command unit buffer RAM 516*);

a memory device storing rendering information (c. 9 ll. 28-30: *Main processor 100 stores the texture images 116 into main memory 300 for access by display processor 500*; c. 13 ll. 44-60: *Main memory 300 provides ... display list graphics commands 110a, texture maps 116 and other graphics data 112c; color image frame buffer 118a, and coprocessor working values*), the memory device accessible in response to the generate_event command (c. 52 ll. 32-38: *load tile command*); and

the command queue capable of queuing the rendering commands (Fig. 20: *command unit buffer RAM 516*) .

5. Van Hook discloses that the DMA controller 518 reads a string of graphics display commands from main memory (Fig. 20 and c. 48 ll. 7-16), and that the display processor 500 accesses main memory 300 via memory interface 512 and coprocessor main internal bus 214, where the memory interface is primarily used to access the color frame buffer and the z buffer (c. 47 ll. 65-c. 48 ll. 6). Van Hook does not expressly teach the direct memory access device is capable of receiving a memory access command in response to the generate_event command. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the DMA controller in Van Hook's system to load texture data from the main memory into the texture memory, instead of the memory interface 512. One would have been motivated to have done so in order to load the data faster and without competing with accesses to the color frame buffer and z buffer.

6. Van Hook discloses that texture loads after primitive rendering should be preceded by a sync load command; but Van Hook does not expressly teach a wait_until command, wherein the wait_until command corresponds to the completion of an operation indicated by the generate_event command, or queuing the rendering commands until the completion of the operation indicated by the generate_event command. Migdal discloses a computer system implementing a synchronization scheme in which texture downloads are synchronized with drawing primitives that use the texture data (c. 11 ll. 35-37). Migdal discloses that for a texture download followed by drawing commands that use the new texture data, a SetSyncID(g, i) command is issued after the texture download, and a WaitSyncID(g, i) is issued before the first drawing command that uses the texture data; and for drawing commands followed by a texture download that overwrites old texture data, a SetSyncID(g, j) command is issued after the last drawing command that uses the old texture data, and a WaitSyncID(g, j) command is issued before the texture download in order to guarantee proper synchronization (c. 11 ll. 37-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the SetSyncID(g, i) command and the WaitSyncID(g, i) command as taught by Migdal in combination with Van Hook's texture load command and the command unit buffer RAM, in order to synchronize the texture downloads with the drawing primitives that use the texture data as taught by Migdal.

7. As per claim 2, Van Hook discloses that the memory device is an external memory device, the apparatus further comprising: the external memory device storing a plurality of rendering data sets (Fig. 5: *main memory 300 storing textures 116, frame buffer 118 and*

graphics database112); and an embedded memory device capable of storing one of the plurality of rendering data sets (Fig. 5: *texture memory 502 within display processor 500*).

8. As per claim 3, Van Hook discloses that the memory access command includes loading one of the plurality of rendering data sets from the external memory to the embedded memory (c. 48 ll. 27-30: *display processor 500 obtains data for its texture memory 502 by passing texture load commands to command unit 514 and using memory interface 512 to perform those commands*).

9. As per claim 4, Van Hook discloses that the embedded memory includes a plurality of memory portions and the plurality of rendering data set is loaded to one of the plurality of memory portions (c. 51 ll. 1-14: *texture memory is divided into four simultaneously accessible banks, giving output of four texels per clock cycle. Video game program 58 can load varying-sized textures with different formats anywhere in the texture memory 502*).

10. As per claim 6, Van Hook discloses a graphics rendering engine operably coupled to the command queue such that the graphics rendering engine generates the rendering commands, the generate_event command (Fig. 20: *display processor 500 comprising the command unit buffer RAM 516*).

11. As per claim 7, Van Hook discloses a command processor, coupled to the command queue and the direct memory access device such that the processor executes the rendering commands (Figs. 5 & 20: *display processor 500 comprising the command unit buffer RAM 516, DMA controller 518, rasterizer 504, texture unit 506, color combiner 508, and blender 510*).

12. As per claim 8, Van Hook discloses that the rendering commands include accessing the rendering information in the memory device (Fig. 18: *display processor processing includes accessing textures for texture mapping*).

13. As per claim 9, Van Hook discloses that the generate_event command includes a pointer such that upon completion of the event, the pointer is provided to the command queue (c. 52 ll. 32-40: *The "load tile" command is used to load a tile into texture memory 502*; Fig. 57: *Load_Tile command includes tile descriptor index*; c. 51 ll. 8-11: *Texture coordinate unit 530 maintains eight texture tile descriptors that describe the location of texture images within texture memory 502*).

14. Claims 10, 11, 13, 15, 16, 17 are similar in scope to claims 1-4 and 6-9, and are rejected under the same rationale.

15. As per claim 12, Van Hook discloses using the event flag to indicate the completion of the memory operation (Fig. 21D and c. 48 ll. 43-61: *command unit 514 includes a status/command register 534 that acts as a status register indicating whether texture memory 502 is busy (field 536(5); whether the display processor pipeline is busy (field 536(6); whether command unit 514 is busy (field 536(7); whether the command buffer RAM 516 is ready to accept new inputs (field 536(8); whether DMA controller 518 is busy (field 536(9); and whether the start and end addresses and registers 518a and 518b respectively valid (fields 536(10), 536(11)*).

16. As per claim 19, Van Hook discloses that the display processor 500 and the main processor 100 are coupled over a communication path 102 (Fig. 2). Van Hook does not expressly teach a flex cable, or mounting a graphics rendering chip on the flex cable as per claim

20. To one of ordinary skill in the art, commonly having the knowledge that flex cables are utilized to internal connections, it would have been obvious at the time the invention was made, to have implemented the communication path 102 as a flex cable. Additionally, as Applicant admits that flex mounting techniques are well known, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have mounted Van Hook's display processor on the flex cable.

17. As per claim 21, Van Hook discloses that the graphics rendering chip operable coupleable to at least one display such that command processor upon generating a video display output, the video display output may be provided to the at least one display (Fig. 5: *display processor outputs to display 58*).

18. As per claim 23, Van Hook discloses that the rendering information is at least one of: texture data vertex data and scene description data (Fig. 5: *texture memory 502 and main memory storing texture data 116 and display list 110*).

19. Claims 5, 14, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,342,892 to Van Hook et al and U.S. Patent No. 6,762,763 to Migdal et al and U.S. Patent No. 6,609,977 to Shimizu et al.

20. As per claims 5, 14, and 18, Van Hook does not expressly teach that the external memory is a secure digital memory card. Shimizu, in an analogous art, teaches system interfaces used to connect graphics system to audio, video, mass media storage device, communications, and other electronic devices (c. 1 ll. 20-27), in which the system supports SD-memory cards offering large capacity non-volatile storage (Fig. 28B: *memory cards C*). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to have implemented Shimizu's SD-digicard adapter in Van Hook's system in order to provide additional non-volatile storage.

21. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,342,892 to Van Hook et al and U.S. Patent No. 6,762,763 to Migdal et al and U.S. Patent No. 6,677,967 to Sawano et al.

22. As per claim 22, Van Hook does not expressly teach a camera such that a capture video image may be received and processed by the command processor. Sawano, in an analogous art, teaches a video game system in which image data supplied from a video camera are captured and combined with predetermined image data to create and display a combined image (c. 1 ll. 10-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized image capture from a video camera as taught by Sawano in combination with Van Hook's system in order capture video images that are then combined with other images and displayed such that the user's gaming experience is enhanced.

23. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,342,892 to Van Hook et al and U.S. Patent Application Publication No. 2004/0223614 to Seaman.

24. As per claim 24, Van Hook a high performance 3D graphics system comprising:

a central processing unit operably coupled to a processing unit memory module (Figs. 2 & 5: *main processor 100 coupled to the main memory 300*);

a video display controller operably coupled to the central processing unit (Figs. 2 & 5: *main processor 100 coupled to the display processor 500*);

a video display unit coupled to the video display controller such that a video display output may be provided to the video display unit by the video display controller (Figs. 2 & 5: *display 58 coupled to the display processor 500*);

a graphics rendering chip coupled to the central processing unit, wherein the graphics rendering chip includes an embedded memory device, a direct memory access device and an external memory interface (Figs. 5 and 20: *display processor 500 coupled to the main processor 100. The display processor comprises texture memory 502, DMA controller 518, and memory interface 512*); and

an external memory device operably coupleable to the graphics rendering chip across the external memory interface (Figs. 5 and 20: *main memory 300 coupled to the display processor 500 via memory interface 512*), wherein the external memory device stores at least one of a plurality of rendering data sets (Figs. 5: *main memory 300 stores texture data*) that may be provided to the embedded memory (c. 48 ll. 27-30: *display processor 500 obtains data for its texture memory 502 by passing texture load commands to command unit 514 and using memory interface 512 to perform those commands*) for the processing of the video display output by the graphics rendering chip such that the video display output may be provided to the video display controller (c. 44 ll. 64-66: *display processor 500 rasterizes triangle and rectangles and produces high quality pixels that are textured, anti-aliased, and z-buffered*).

25. Van Hook does not expressly teach a baseband receiver operably coupled to a wireless antenna. Seaman teaches a system for receiving secure video comprising RF transceiver 120 and antenna 111 (Figs. 1 and 2) and that is utilized for providing video gaming services ([0042],

[0064], and [0065]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the wireless transceiver and antenna as taught by Seaman in combination with Van Hook's system in order to provide interactive video gaming services to the user to enhance the user's experience.

26. As per claim 25, Van Hook discloses that the display processor 500 and the main processor 100 are coupled over a communication path 102 (Fig. 2). Van Hook does not expressly teach a flex cable, or mounting a graphics rendering chip on the flex cable. To one of ordinary skill in the art, commonly having the knowledge that flex cables are utilized to internal connections, it would have been obvious at the time the invention was made, to have implemented the communication path 102 as a flex cable. Additionally, as Applicant admits that flex mounting techniques are well known, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have mounted Van Hook's display processor on the flex cable.

27. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,342,892 to Van Hook et al and U.S. Patent Application Publication No. 2004/0223614 to Seaman and U.S. Patent No. 6,609,977 to Shimizu et al.

28. As per claim 26, Van Hook does not expressly teach that the external memory is a secure digital memory card. Shimizu, in an analogous art, teaches system interfaces used to connect graphics system to audio, video, mass media storage device, communications, and other electronic devices (c. 1 ll. 20-27), in which the system supports SD-memory cards offering large capacity non-volatile storage (Fig. 28B: *memory cards C*). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to have implemented Shimizu's SD-digicard adapter in Van Hook's system in order to provide additional non-volatile storage.

29. Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,342,892 to Van Hook et al and U.S. Patent Application Publication No. 2004/0223614 to Seaman and U.S. Patent No. 6,762,763 to Migdal et al.

30. Claims 27 and 28 are similar in scope to claims 1-4 and 6-9, and are rejected under the same rationale.

31. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,342,892 to Van Hook et al and U.S. Patent Application Publication No. 2004/0223614 to Seaman and U.S. Patent No. 6,677,967 to Sawano et al.

32. Claim 29 is similar in scope to claim 22 and is rejected under the same rationale.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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US006201547B1

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka J. Chauhan whose telephone number is 571-272-7782. The examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
March 18, 2005